Technical Specification for LPC-SPI Bridge

Table of Contents

List Of Figures

List Of Tables

1 Introduction

1.1 Purpose

This document describes the Technical Specification of the LPC-SPI bridge core. It includes the overall architectural description, detailed functional specifications and interface definitions for the LPC-SPI bridge.

1.2 Features

The following are the main features of the LPC-SPI bridge:

- LPC Bus interface:
  - Compliant with Intel's LPC interface specification Revision 1.1.
  - Supports LPC bus cycle types : Memory, I/O, and Firmware Memory
  - Support for LPC slave interface.
  - Synchronous 33MHz bus clock cycles.
  - Multiplexed Command, Address and Data Bus
  - Supports 8-bit transfer size.
- SPI Bus interface:
  - Supports SPI master mode
  - Supports Full duplex mode .
  - Supports one SPI slave select line
  - Serial clock with programmable polarity and phase
  - Supports Interrupt generation

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
LPC	Low pin count
SPI	Serial peripheral interface
FPGA	Field Programmable Gate Array
FSM	Finite State machine
LSB	Least Significant Byte
MSB	Most Significant Byte

2 LPC-SPI Bridge

2.1 Block Diagram

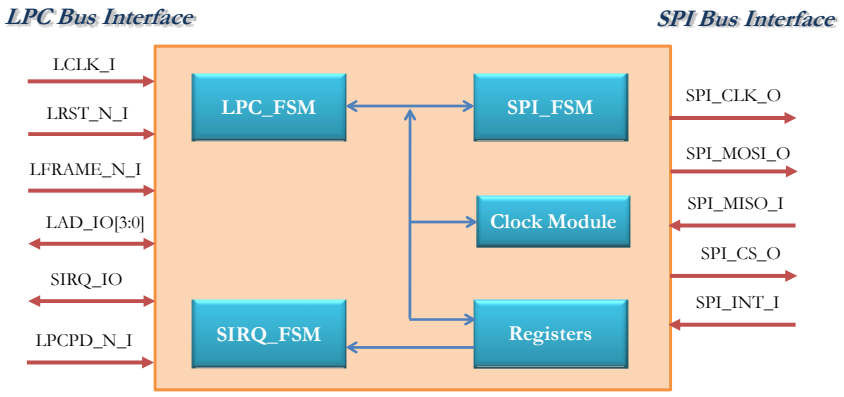

Figure 1 LPC-SPI Bridge Diagram

2.2 Description

The main blocks in LPC-SPI Bridge are

- **LPC FSM:** This implements LPC state machine's whose primary function is to receive read or write requests from the LPC bus, store the address, data ,start the SPI state machine and turn the control back to the LPC host. It is driven from the LCLK_I input of LPC host with each state represents clock cycles in compliance with the LPC specification**.**
- **SPI FSM:** The SPI state machine's primary function is to transmit the command ,address and data to the SPI slave device, store the data returned from the SPI slave device, and transmit the data to the LPC host over the LPC bus.
- **SEIRQ FSM:** The SEIRQ state machine is responsible for transferring interrupt request from SPI device to the LPC host controller. SEIRQ cycles consists of three frame types: start frame, SEIRQ frame and stop frame.
- **CLOCK MODULE:** Clock module will generate the SPI output clock for the SPI slave device based on the clock selection bits of the SPI control register.
- **REGISTERS:** The SPI registers are SPI control register and SPI status register. SPI registers are accessed using LPC IO write/read cycles.

2.3 I/O Signal Description

Table 2: LPC Interface IO Signal Description

Signal	I/O	Width	Description
LRST_N_I	I	1	System Reset. Active Low Asynchronous reset input from the LPC host
LCLK_I	I	1	System Clock. 33MHz Clock input to the FPGA.
LFRAME_N_I	I	1	Indicates start of a new cycle, termination of broken cycle
LAD_IO[3:0]	IO	4	Multiplexed Command, Address, and Data
SEIRQ_IO	IO	1	Needed by peripherals that need interrupt support
LPCPD_N_I	I	1	Indicates that the peripheral should prepare for power to be removed from the LPC I/F devices

Table 3: SPI Interface IO Signal Description

Signal	I/O	Width	Description
SPI_CLK_O	I	1	Clock output with respect to which the SPI transfers data
SPI_CS_N_O	I	1	Output the select signal from the SPI module to another peripheral with which a data transfer is to take place

Signal	I/O	Width	Description
SPI_MOSI_O	O	1	Transmit data out of the SPI module
SPI_MISO_I	I	1	Receive data in from the SPI slave module
SPI_INT_I	I	1	External interrupt from the SPI device

3 Register Description

3.1 Register List

The Register list of the LPC-SPI Bridge is as shown in Table 44 below.

These Registers can be accessed by the LPC Host using IO read or write cycles.

Table 4: Register List

Sl.No	Register Name	Description
	SPI registers	
1.	SPI Control Register	Read or written at any time, is used to configure the SPI system
2.	SPI Status Register	Contains interrupt status flag indicating the completion of an SPI transfer

4 Timing Waveforms

4.1 LPC Interface

4.1.1 Memory read Cycle

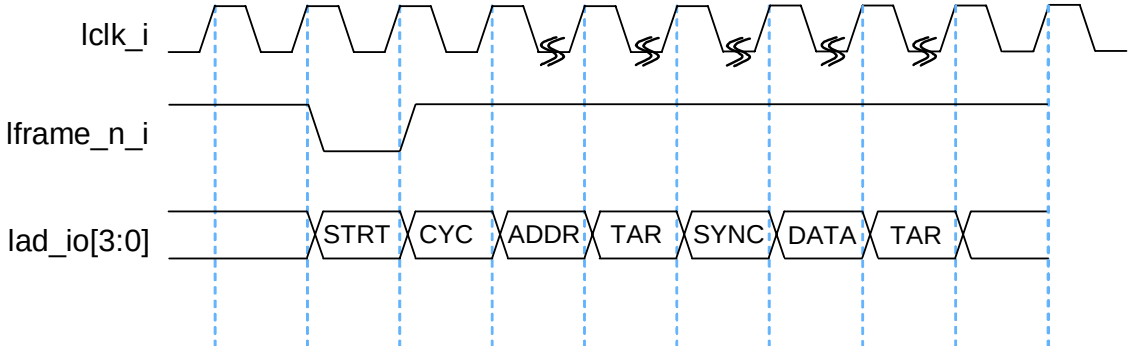

Figure 2: LPC Interface memory read Timing Diagram

4.1.2 Memory Write Cycle

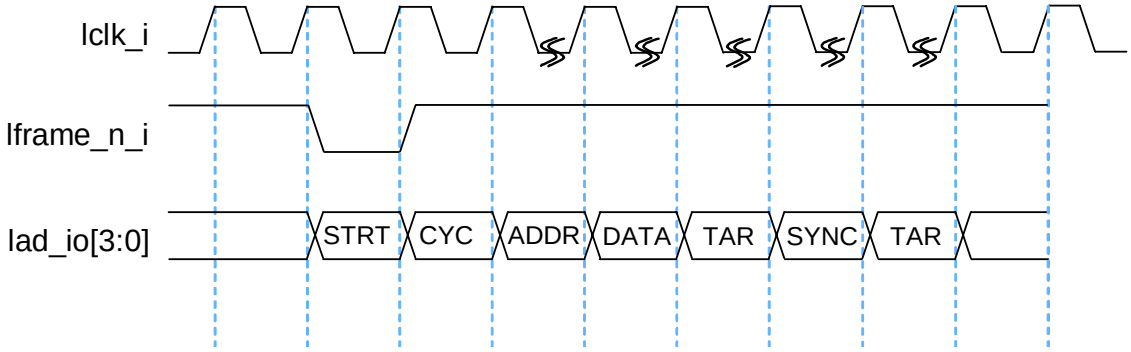

Figure 3: LPC Interface memory write Timing Diagram

4.1.3 IO Read Cycle

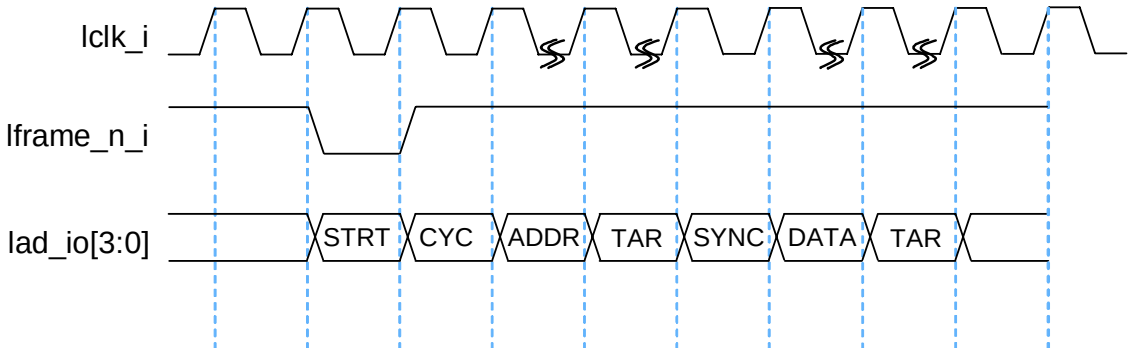

Figure 4: LPC Interface IO read Timing Diagram

4.1.4 IO Write Cycle

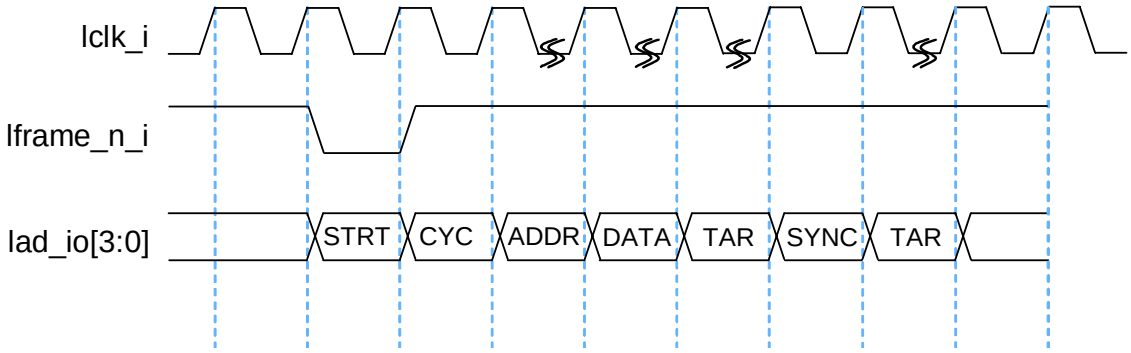

Figure 5: LPC Interface IO write Timing Diagram

4.1.5 Firmware Memory Read Cycle

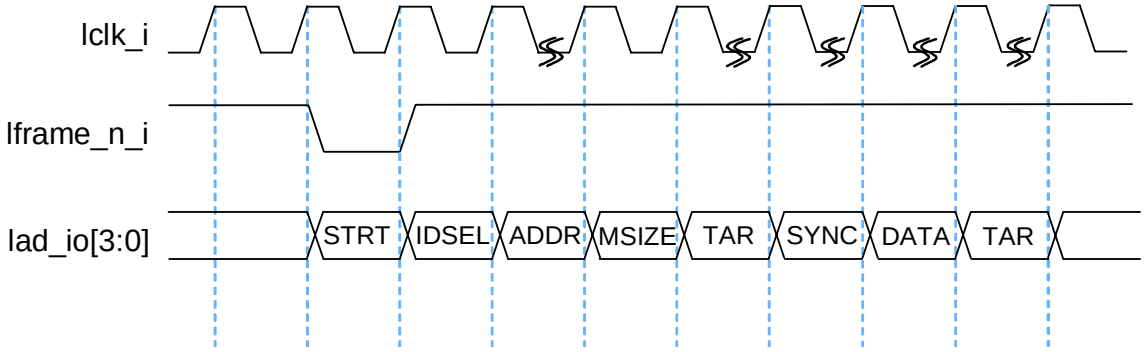

Figure 6: LPC Interface Firmware Memory Read Timing Diagram

4.1.6 Firmware Memory Write Cycle

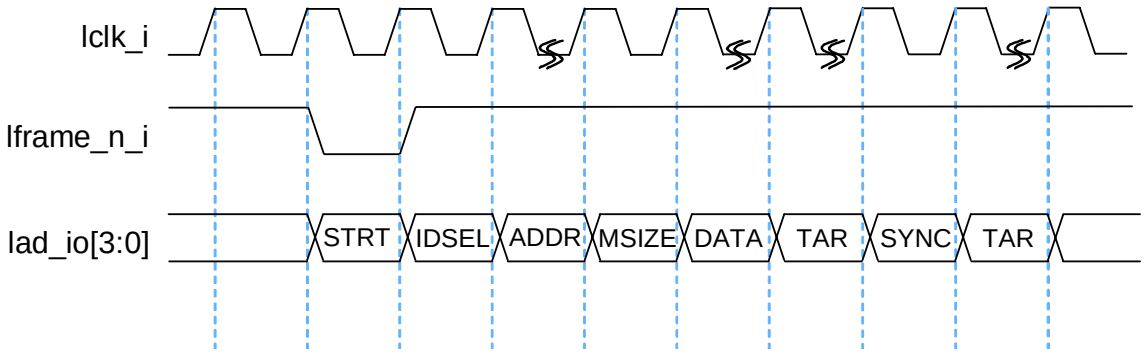

Figure 7: LPC Interface Firmware Memory write Timing Diagram

4.2 SPI Interface

4.2.1 SPI data transfer Cycle with cpha =0

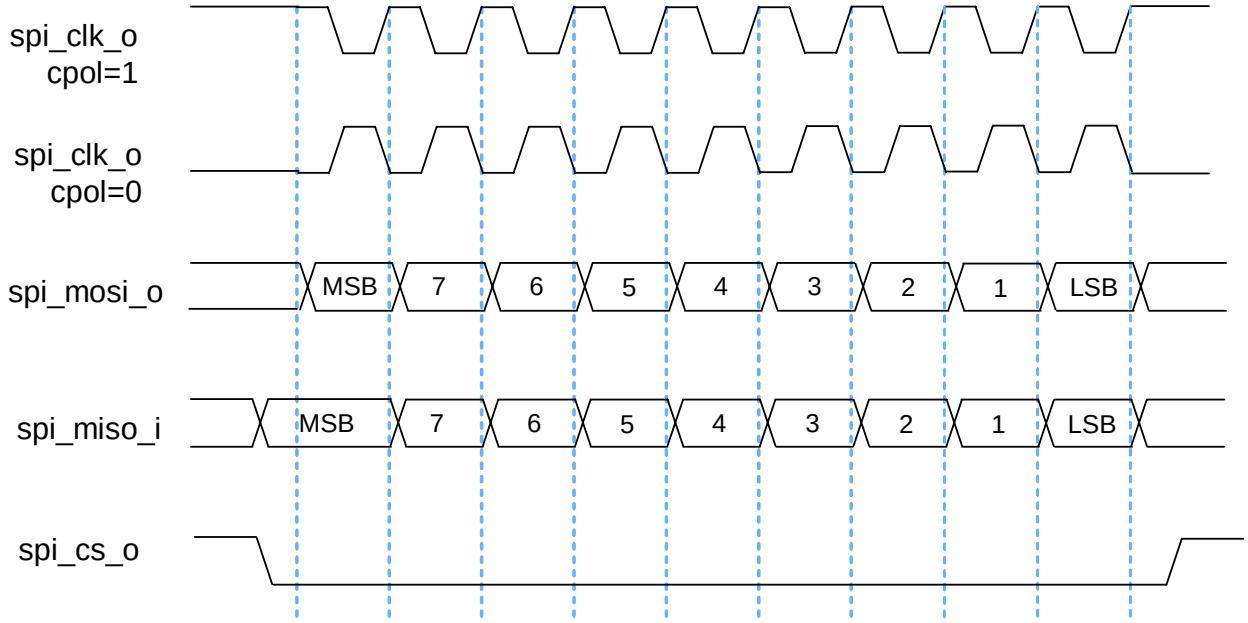

Figure 8: SPI data transfer cycles with cpha=0 Timing Diagram

4.2.2 SPI data transfer Cycle with cpha =1

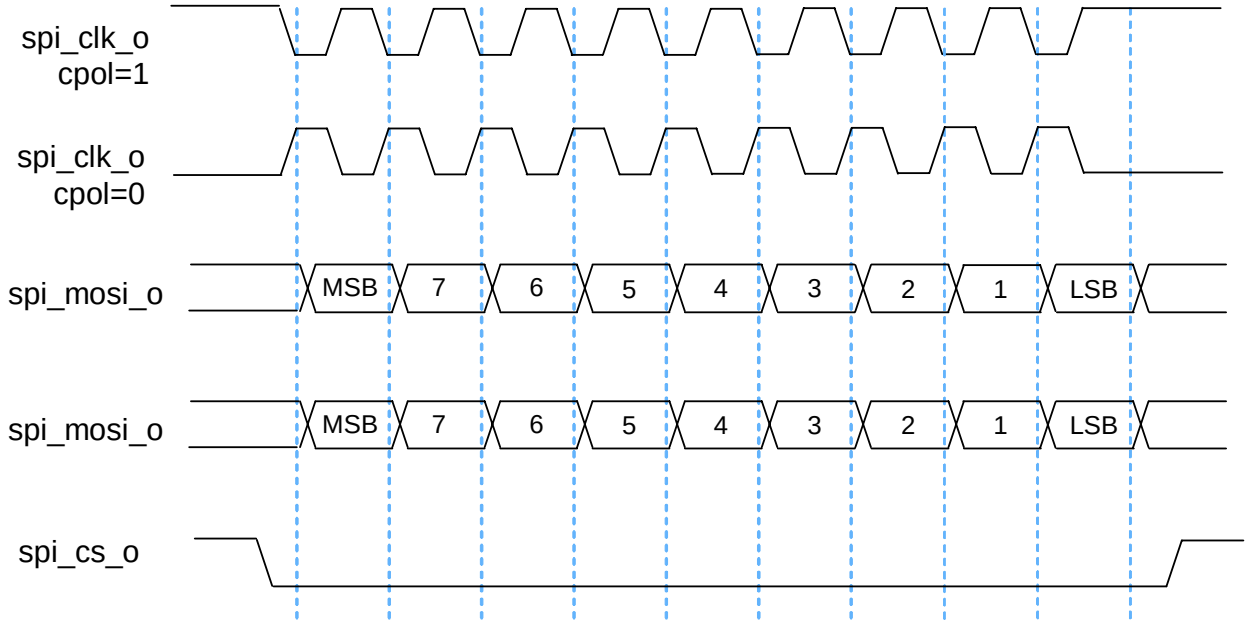

Figure 9: SPI data transfer cycles with cpha=1 Timing Diagram